In the Claims:

1. (Currently Amended) A microprocessor comprising:

a processing unit;

a memory connected to said processing unit and comprising an addressable memory space for a lower memory area and an extended memory area;

means for connecting to and accessing said addressable memory space;

means for executing instructions of an instruction set executable by said processing unit, the instruction set comprising instructions for accessing said addressable memory space, ~~the instruction set comprising~~ a first instruction group comprising instructions for accessing said lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the ~~for gathering~~ instructions ~~in the instruction set~~ for accessing said extended memory area; and

means for preventing access to said extended memory area when executing an instruction in the first instruction group.

2. (Currently Amended) A microprocessor according to Claim 1, wherein each location in said addressable memory space is associated with a respective access address; and further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group.

3. (Original) A microprocessor according to Claim 1, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

4. (Original) A microprocessor according to Claim 1, wherein each location in said addressable memory space is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area, the microprocessor further comprises means for maintaining an address of a jump destination location so that it points to a location in said lower memory area.

5. (Original) A microprocessor according to Claim 1, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area; and further comprising means for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area.

6. (Original) A microprocessor according to Claim 1, wherein the second instruction group comprises instructions for accessing said extended memory area in an indirect addressing mode.

7. (Original) A microprocessor according to Claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area.

8. (Original) A microprocessor according to Claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area.

9. (Original) A microprocessor according to Claim 1, wherein said means for connecting to and accessing said addressable memory space comprises an address bus; and further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space.

10. (Original) A microprocessor according to Claim 1, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

11. (Currently Amended) A microprocessor comprising:

a processing unit;

a memory connected to said processing unit and comprising an addressable memory space for a lower memory area and an extended memory area;

an address bus connected to said memory; ~~and~~

an instruction set ~~for accessing said addressable memory space~~ executable by said processing unit, the instruction set comprising

a first instruction group comprising instructions for accessing said lower memory area, and

a second instruction group distinct from the first instruction group ~~for gathering~~ and only comprising all of the instructions ~~in the instruction set~~ for accessing said extended memory ~~area,~~ area; and

~~instructions~~ means for preventing access to said extended memory area when executing an instruction in the first instruction group.

12. (Currently Amended) A microprocessor according to Claim 11, wherein each location in said addressable memory space is associated with a respective access address; and ~~wherein said instruction set~~ further ~~comprises instructions~~ means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group.

13. (Original) A microprocessor according to Claim 11, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary

memory location and said at least one internal register.

14. (Original) A microprocessor according to Claim 11, wherein each location in said addressable memory space is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area, said instruction set further comprises instructions for maintaining an address of a jump destination location so that it points to a location in said lower memory area.

15. (Original) A microprocessor according to Claim 11, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area; and wherein said instruction set further comprises instructions for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area.

16. (Original) A microprocessor according to Claim 11, wherein the second instruction group comprises instructions for accessing said extended memory area in an indirect addressing mode.

17. (Original) A microprocessor according to Claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area.

18. (Original) A microprocessor according to Claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area.

19. (Original) A microprocessor according to Claim 11, further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space.

20. (Original) A microprocessor according to Claim 11, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

21. (Currently Amended) A method for accessing a memory used by a microprocessor, the microprocessor comprising a processing unit, an address bus connected to the processing unit, with the memory being connected to the address bus and comprising an addressable memory space for a lower memory area and an extended memory area, the method comprising:

executing an instruction for accessing the lower memory area, the instruction belonging to an instruction set comprising a first instruction group comprising instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area;

~~accessing the lower memory area using a first instruction group;~~

~~gathering instructions in the instruction set for accessing the extended memory area; and~~

preventing access to the extended memory area when executing the first instruction group.

22. (Currently Amended) A method according to Claim 21, wherein each location in the addressable memory space is associated with a respective access address; and further comprising ~~instructions for~~ forcing an access address of a location to be accessed to point to a location in the lower memory area when executing an instruction in the first instruction group.

23. (Currently Amended) A method according to Claim 21, wherein the microprocessor further ~~comprising~~ comprises at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in the addressable memory space; and

data transfer instructions between the arbitrary memory location and the at least one internal register.

24. (Original) A method according to Claim 21, wherein each location in the addressable memory space is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in the lower memory area, further comprising maintaining an address of a

jump destination location so that it points to a location in the lower memory area.

25. (Original) A method according to Claim 21, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in the lower memory area; and further comprising forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in the lower memory area and points to this area.

26. (Original) A method according to Claim 21, wherein the second instruction group comprises instructions for accessing the extended memory area in an indirect addressing mode.

27. (Original) A method according to Claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located in the lower memory area.

28. (Original) A method according to Claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located within the extended memory area.

29. (Original) A method according to Claim 21, wherein the microprocessor further comprises a program pointer register having a size corresponding to a size of the address bus for enabling access to a program instruction to be

executed that is located at an arbitrary location in the addressable memory space.

30. (Original) A method according to Claim 21, wherein the lower memory area is accessible over 16 bits and the extended memory area is accessible over 24 bits.